REMARKS

At the time the current Official Action was mailed, the Examiner rejected claims 1-13, 15-36, and 38-40, and objected to claims 14 and 37. Claims 1-40 remain pending. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Rejections under 35. U.S.C. § 102

The Examiner rejected claims 1-8, 13, 15-17, and 21-30 under 35 U.S.C. § 102 as being anticipated by Khosrowpour (U.S. 6,202,115). Specifically, the Examiner stated:

> Claims 1-8, 13, 15-17 and 21-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Khosrowpour (U.S. Pat. No. 6,202,115).
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> With regard to claims 1-8, 13, 15-17 and 21-30, Khosrowpour shows a bus bridge system and a method thereof comprising a processor (as in computer network, col. 1, line 13), a memory device (Fig. 1) coupled to the processor including a first voltage bus (101), a second voltage bus (102), a bridge circuit (110, 120) coupled between the first voltage bus and the second voltage bus for receiving an input signal (112, 122) such as connecting the first voltage bus to the second voltage bus if the input signal is a first control signal (112) and isolating the first voltage bus from the second voltage bus if the input signal is a second control signal (122) (see col. 4, lines 14-27, noting that first and second control signals 112, 122 as in drawings, but mistakenly listed as 115 and 125, respectively), the memory device further including a DRAM device and SRAM device (col. 5, line 21), the processor being coupled to a communication port to communicate with an input/output device, to a user interface, or to a display presenting information to a user, and to the power supply being externally to the memory, the first voltage being a voltage supply bus for periphery circuitry and the second voltage bus being a voltage supply bus for array circuitry (col. 1, lines 11-50, col. 2, lines 28-68).
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> Office Action, pages 2-3.

Applicants respectfully traverse this rejection. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v.*

Banner, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

The present application relates to the distribution of power in sections of semiconductor devices, such as a memory chips. Memory chips may be divided into array circuitry and periphery circuitry sections, for example. *See* p. 9, ll. 20-22. The array circuitry may include memory banks for DRAM, SRAM, or other memory types. *See* p. 9, ll. 22-23. The periphery circuitry may include circuitry and other structures used to support the array section, such as drivers, interconnects between circuitry, decoders, or other similar circuitry. *See* p. 9, ll. 23 to p. 10, ll. 2. As explained in the application, improvements in power distribution may reduce the power consumed by the memory, as well as provide faster access to the information stored in the memory. *See* p. 9, ll. 10-13.

To properly distribute power, a bridge circuit connects or isolates voltage buses. *See* p. 6, ll. 1-7. The bridge circuit may act as a short during certain modes to allow the array and periphery sections to share components, such as amplifiers. *See* p. 12, ll.13-18. Alternatively, the bridge may isolate the sections to prevent noise interference to couple between the sections. *See* p. 14, ll. 17-19. Thus, effective power distribution within a memory chip is accomplished by selectively coupling or isolating the voltage buses of the array and periphery sections. To

accomplish this task, the bridge circuit is configured to isolate the voltage buses, or connect the voltage buses depending on the control signal received by the bridge circuit. *See* p. 23, l. 19 to p. 24, l. 6.

As such, independent claim 1 recites, *inter alia*, "A system comprising: a bridge circuit...wherein the bridge circuit is adapted to... connect the first voltage bus and the second voltage bus together if the input signal is a first control signal; and isolate the first voltage bus from the second voltage bus if the input signal is a second control signal." Independent claim 15 recites, *inter alia*, "A memory device comprising... a bridge circuit...wherein the bridge circuit is configured to... connect the periphery voltage bus and the array voltage bus together if the input signal is a first control signal; and isolate the periphery voltage bus from the array voltage bus if the input signal is a second control signal." Independent claim 24 recites, *inter alia*, "A method of operating a device comprising the acts of... receiving a control signal at a bridge circuit... coupling the periphery voltage bus to the array voltage bus if the control signal indicates the first condition; and isolating the periphery voltage bus from the array voltage bus if the control signal indicates the second condition." Therefore, each of the independent claims 1, 15, and 24 sets forth a bridge circuit that couples or isolates voltage buses according to a control signal.

In sharp contrast, Khosrowpour does not disclose a bridge circuit that couples or isolates voltage buses according to a control signal. Khosrowpour is directed to providing bus redundancy for fail-over and data preservation purposes. *See* col. 6, ll. 23-49. Specifically,

Khosrowpour discloses a system having first and second buses and bridges where data is cached in first and second caches. *See* col. 6, ll. 23-33. In the event that failure in a bridge occurs, data may still be available through the other bus via the other cache. *See* col. 6, ll. 34-49. The bridges in Khosrowpour do not, however, connect or isolate voltage buses in response to a control signal as set forth in claims 1, 15, and 24, and thus, cannot possibly anticipate the recited subject matter. As such, Khosrowpour does not disclose each element of the independent claims 1, 15, and 24. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of independent claims 1, 15, and 24, as well as all claims dependent thereon.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 9, 10, 18, 19, 31, 33, 36, and 38-40 under 35 U.S.C. § 103(a) as being unpatentable over Khosrowpour in view of Nakagawa et al. (US 6,643,713). In addition, the Examiner rejected claims 11, 12, 20, and 32 under 35 U.S.C. § 103(a) as being unpatentable over Khosrowpour in view of Liu (US 6,940,340). Additionally, the Examiner rejected claims 34 and 35 under 35 U.S.C. § 103(a) as being unpatentable over Khosrowpour in view of Nakagawa et al. as applied to claim 33, and further in view of Liu. With regard to independent claim 33, the Examiner stated:

> Claims 9, 10, 18, 19, 31, 33, 36 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowour in view of Nakagawa et al. (U.S. Pat. No. 6,643,713).
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> With regard to claims 9, 10, 18, 19, 31, 33, 36 and 38-40, Khosrowpour shows a bus bridge system and a method thereof comprising all the claimed subject matter as discussed in the subparagraph 2 above, except for a plurality of power amplifiers coupled to the first voltage bus. Nakagawa et al. (Fig. 2) disclose an internal connection for a

> communication system in which a power amplifier (212) is included. It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the power amplifier as shown in Nakagawa et al. into the bus bridge system of Khosrowpour for the purpose of enhancing the power to the voltage bus.
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> Office Action, page 3.

Applicants respectfully traverse this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985).

As discussed in detail above, the present application is directed to distributing power in a semiconductor device. Through proper distribution of power, the performance of a semiconductor chip, such as a memory chip, may be enhanced. *See* p. 6, ll. 5-7. To this end, independent claim 33 recites, *inter alia*, "A method of manufacturing a memory device comprising the acts of...coupling a bridge circuit to the first voltage bus and the second voltage bus; encoding the memory device to provide a first control signal that couples the first voltage bus to the second voltage bus in response to a first condition; and encoding the

memory device to provide a second control signal that isolates the first voltage bus from the second voltage bus in response to a second condition."

In contrast, Khosrowpour does not disclose encoding a memory device to provide control signals that couple or isolate voltage buses in response to conditions. Khosrowpour is directed to providing bus redundancy for fail-over and data preservation purposes, as discussed earlier. Specifically, Khosrowpour discloses a system having a first and second buses and bridges where data is cached in first and second caches. *See* col. 6, ll. 23-33. In the event that failure in a bridge occurs, data may still be available through the other bus via the other cache. *See* col. 6, ll. 34-49. Contrary to the Examiner's assertion, however, Khosrowpour does not disclose encoding a memory device to provide control signals that couple or isolate voltage buses in response to conditions, as set forth in claim 33. As such, Khosrowpour fails to disclose all the elements of independent claim 33.

Nakagawa fails to obviate the deficiencies of Khosrowpour. Nakagawa is directed to a mobile communication system having a DSP/CPU integrated chip. *See* col. 1, ll. 14-20; col. 5, ll. 11-15. Specifically, Nakagawa describes a system where the DSP and CPU share RAM and ROM to reduce the number of buses, signal lines and memory chips necessary. *See* col. 10, ll. 65 to col. 11, ll. 8. The result is a small, low cost and low power consumption mobile communication terminal. *See* col. 11, ll. 4-8. Nakagawa does not, however, disclose encoding a memory device to provide control signals that couple or isolate voltage buses in response to conditions, as set forth in claim 33. As such, Nakagawa does not disclose all the elements of claim 33 and fails to obviate the deficiencies of Khosrowpour. Accordingly, Applicants

respectfully submit that Khosrowpour and Nakagawa, either alone or in combination, fail to disclose or suggest all the elements of independent claim 33.

In light of the foregoing discussion, Applicants respectfully assert that none of the references, alone or in combination, render the recited subject matter obvious. Accordingly, Applicants respectfully request the withdrawal of the rejection and allowance of independent claim 33, as well as all claims depending thereon. Additionally, Applicants respectfully request withdrawal of the rejections of all other dependent claims rejected under 35 U.S.C. §103 based on their dependency on allowable claims.

Allowable Subject Matter

In the Office Action, the Examiner indicated that claims 14 and 37 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for indicating claims 14 and 37 as containing allowable subject matter. In light of the forgoing discussion, however, the Applicants have chosen not to amend the claims as they are believed to be allowable as originally filed.

Conclusion

In view of the remarks set forth above, Applicants respectfully requests reconsideration of the Examiner's rejections and allowance of all pending claims. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Authorization for Extensions of Time and Payment of Fees

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request thereof. The Commissioner is authorized to charge any requisite fees which may be required to Deposit Account No. 06-1315; Order No. MICS:0119/FLE.

Respectfully submitted,

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